REMARKS

Claims 1-4, 6-13, 15-20, 22-25, 27-35 are currently pending. Claims 1, 10, 20 and 25 have been amended. Claims 5, 14, 21 and 26 have been canceled.

The Examiner has stated " The proposed drawings, filed on October 15, 2002 have been approved. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance." In response, Applicants submitted corrected drawings with this response..

The Examiner rejected claims 1-4, 6-13, 15-20, 22-25, 27-29 under 35 U.S.C. §103(a) as being unpatentable over Farrar (US 6,376,370 B1) in view of Haveman (US 6,156,651).

The Examiner rejected claims 30-33 under 35 U.S.C. §103(a) as being unpatentable over Farrar (US 6,376,370 B1) in view of Otsuka et al. (US 6,1373, 136 B2).

The Examiner rejected claims 34 and 35 under 35 U.S.C. §103(a) as being unpatentable over Farrar et al. (US 6,376,370 B1) in view of Otsuka et al. (US 6,1373, 136 B2) as applied to claims 31 and 33 above, and in further view of Havemann (Us 6,156,651)..

Applicants respectfully traverse the §103 rejections with the following arguments.

35 USC § 103

As to claims 1-4, 6-13, 15-20, 22-25, 27-29 the Examiner states that "Farrar shows (fig. 3K) an interconnect structure comprising a lower level in a dielectric layer having a side and bottom, the lower level wiring comprising a core conductor (307B and 320) and a lower conductive liner (306B and 314)."

Applicants can not find 320 in any FIG. of Farrar. Therefore, Applicants are unable to understand the structural relationship the Examiner is citing as the basis of his rejection or

determine what elements the Examiner has related to elements of Applicants invention and thus are unable to fully respond to the Examiners rejection. Applicants request further clarification on this issue.

The Examiner further states "The lower level wire also has integral extensions (part above 307), the extensions having a side and a bottom, wherein the lower level wire and extensions also comprise the lower core conductor (320) and the lower conductive liner (314). The liner is formed on the side and bottom of the lower level wire and the extension. The lower conductive liner has an upper edge having an inner surface, an outer surface, and a top surface, the top surface of the upper edge substantially coplanar with a top surface of the dielectric layer. The interconnect also comprises an upper level wire (330) having a side and bottom and a via integrally formed in the bottom of the upper level wire. The via also has a side and bottom. The upper level wire and via comprise an upper core conductor (344) and an upper conductive liner (334), which is formed on the side and bottom of the upper level wire and on the side and bottom of the via. The upper conductive liner on the bottom of the via is in contact with the lower core conductor and also in contact with the lower conductive liner in a liner-to-liner contact region. The lower level wire is formed in a lower level dielectric (302 and 308) and upper level wire is formed in an upper level dielectric (324). The upper and lower core conductors comprise copper (col. 17, lines 20-39) and the upper and lower conductive liners comprise tantalum nitride (col. 18, lines 22-23). The lower conductive liner includes an upper edge having an inner surface, an outer surface, and a top surface (top of layer 381 and 382) and the upper conductive line on the bottom of the via contacts one of the top surfaces to form the liner-to-liner contact region. The liner-to-liner contact region also comprises a first portion co-extensive with the lower conductive liner on a portion of a first side (top surface of liner 314) of the lower level wire under the via

(see the interface 319 between 383 and 381). The first and second dielectrics consist of silicon oxide (col. 17, lines 39-47). Farrar shows all the elements of the claims except a portion of the bottom of the upper level wire extending below a top surface of the lower wire level, the upper conductive loner in contact with the inner or outer surface of the upper edge of the conductive liner, and the second and third portions of the liner-to-liner contact region being coextensive with the lower conductive liner. Havemann shows (fig. 3g) an interconnect structure in which a lower level wire has a lower core conductor (39) and a lower conductive liner (36). An upper level wire has an upper core conductor (52) and an upper liner (48), in which the upper liner is in contact with the lower to form a liner-to-liner contact region. A portion of the bottom of the upper level wire extends below a top surface of the lower wire level. The upper conductive liner is in contact the lower core conductor and also in contact with the inner surface of the outer surface or both surfaces of the upper edge of the conductive liner (see how the ipper liner 48 overlaps the upper edge and sides of lower liner 36). The liner-to-liber contact region also comprises a second portion (overlap portion of liner 36) of the lower level wire and a third portion (overlap portion of liner 48 in the hole) co-extensive with the lower conductive liber on an end (inner portion of the liner 36) of the lower level wire, each portion being under the upper level wire. With this configuration, the interconnect can be formed without mechanical defects (abstract). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the liner-to-liner contact region of Farrar by adding the second and third coextensive portions as taught by Havemann to form a contact without mechanical defects."

Applicants contend that claims 1, 10, 20 and 25 are not anticipated by Farrar in view of Havemann because the Examiners statement of the motivation to modify Farrar by Havemann " to form a contact without mechanical defects" is incorrect and not persuasive. Applicants quote

from the Havemann abstract "The conductor metal may be doped with the selectively deposited via metal being doped by dopant diffusion from the conductor metal, thereby avoiding the difficulty of depositing a doped selective metal. Methods are shown for realizing desirable insulating and conducting layers without deleterious mechanical defects." Applicants point out in the Havemann abstract and again in Havemann col. 2, lines 20 to 32 the method of forming "a contact without mechanical defects" as stated by the Examiner applies to a doped metal in the via structure comprising elements 54, 52, 48, 39 ,38 and 36 as illustrated in Havemann FIG. 3. Since Farrar does not utilize a doped via metal. Applicants contend there is no motivation for combining Farrar and Havemann.

Applicants further contend that the Examiner is citing a method of making a contact against a claim to a contact structure which is improper.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 10, 20 and 25 are not unpatentable over Fararr in view of Otsuka et al. and are in condition for allowance. Since claims 2, 3 and 6-9 depend from claim 1, claims 12, 13, 15-19 depend from claim 10, claims 22-24 depend from claim 20 and claims 27-29 depend from claim 25, Applicants contend that claims 2, 3, 6-9, 12, 13, 15-19, 22-24 and 27-29 are also in condition for allowance.

As to claims 30 and 31 (which Applicants note is a repetition the July 17, 2002 action), the Examiner states that "Farrar shows (fig. 3K) an interconnect structure comprising a lower level wire having a side and bottom, the lower level wiring comprising a core conductor (307B and 320) and a lower conductive liner (306B and 314). The liner is formed on the side and bottom of the lower level wire. The interconnect also comprises an upper level wire (330) having a side and bottom and a via integrally formed in the bottom of the upper level wire. The

via also has a side and bottom. The upper level wire and via comprise an upper core conductor (344) and an upper conductive liner (334), which is formed on the side and bottom of the upper level wire and on the side and bottom of the via. The upper conductive liner on the bottom of the via is in contact with the lower core conductor and also in contact with the lower conductive liner in a liner-to-liner contact J. region. The lower level wire is formed in a lower level dielectric (302 and 308) and upper level wire is formed in an upper level dielectric (324). Farrar shows all of the elements of the claims except the dielectric pillars formed in the lower level wire. Otsuka et al. discloses (col. 12, lines 30-52) insulating pillars formed in a level of wiring. With such a configuration a highly reliable damascene structure is formed (col. 2, lines 50-52). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the lower interconnect wiring level of Farrar by adding dielectric pillars as taught by Otsuka et al. to form a highly reliable damascene wiring structure."

The Examiner further stated in response to Applicants arguments of October 15, 2002 concerning claims 30 and 31 "Applicant's arguments filed with respect to claims 30 and 31 have been fully considered but are not persuasive. The applicant primarily argues that Farrar in view of Otsuka et al. does not teach every feature of the claims, specifically that Farrar in view of Otuska et al. does not teach one or more dielectric pillars formed in said lower level wire on the sides of the conductive liner and the upper conductive liner in contact with the lower conductive liner on the sides of the dielectric pillars in a liner-to-liner contact region. The examiner contends that Farrar and Otsuka show all the elements of the claims. Farrar, disclosing the various wiring levels each having conductive cores and liners was only deficient in disclosing dielectric pillars formed in the wiring level. Otsuka was cited to show that conductive pillars were formed in wiring levels to improve the structural integrity. Furthermore, as seen in figure 13C of Otsuka,

the dielectric pillars (P) are formed next to conductive wiring material (10). Therefore one of ordinary skill in the art, wishing to improve the structural integrity of the semiconductor would add the conductive pillars of Otsuka and form them next to the wiring levels having a core and a liner of Farrar. Otsuka thus cures the deficiency of Farrar and shows motivation for the improvement. The 103 rejection is still proper and this action is final."

First, Applicants contend that claims 30 and 31 are not obvious in view of Farrar in view of Otsuka et al. because Farrar in view of Otsuka et al. does not teach or suggest every feature of claims 30 and 31. For example, Farrar in view of Otsuka et al. does not teach or suggest "said lower conductive liner on sides of said dielectric pillars." Applicants maintain that there is no teaching to form a "liner on sides of said dielectric pillars." Applicants contend that the Examiner has assumed formation of a liner on the sides of the pillars absent any teaching or suggestion to do so.

Second, Applicants contend that claims 30 and 31 are not obvious in view of Farrar in view of Otsuka et al. because the Examiners statement of the motivation to modify Farrar by Otsuka et al."to modify the lower interconnect wiring level of Farrar by adding dielectric pillars as taught by Otsuka et al. to form highly reliable damascene wiring structure" is not persuasive. Applicants contend that the improved reliability against void formation taught by Otsuka et al. teaches is not required in Farrar because Farrar already utilizes a different method of improved reliability against void formation. Otsuka et al. teaches in col 3, lines 37 to 43 "With these structures described above, a diameter of crystal grains in the upper wiring above the via hole becomes small so stress migration can be suppressed and wiring disconnections can be reduced. Wiring defects to be caused by stress migration can be suppressed even if a wide wire is formed by using the dual damascene process." Applicants point out that layers 323, 383, 384 of Farrar

already mitigate against stress migration by surrounding the core conductors (copper) with metals not subject to stress migration (tantalum, and tantalum nitride) thus maintaining electrical contact even if voids form in the core conductor. Therefore, there is no need to apply the solution of Otsuka et al. to a problem already solved by Farrar.

Third, Applicants point out that formation of pillars would add an unnecessary expense that Farrar specifically teaches to avoid in col. 2. lines 37 to 42 by stating "If however the lines are made wider, fewer wiring channels can be provided in each metal level. To obtain the same number of wiring channels, additional levels of metal must be provided. This increases the chip cost. So if this approach is to be followed, it is imperative that a low cost process be adopted.," and in col. 4, lines 61 to 62 further stating "What is disclosed herein is a low cost process to achieve reduced capacitance and resistance loss in wiring levels." Applicants contend that addition of the pillars of Otsuka et al. to Farrar are not necessary and add an un-necessary expense.

Based on the preceding arguments, Applicants respectfully maintains that claims 30 and 31 are not unpatentable over Fararr in view of Otsuka et al. and are in condition for allowance. Since claims 32-35 depend from claim 31, Applicants respectfully maintain that claims 32-35 are likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-4, 6-13, 15-20, 22-25, 27-35 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,
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APPENDIX A - IDENTIFICATION OF AMENDED MATERIAL

Claims 1, 10, 20 and 25 are amended herein as follow:

1. (Twice amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom, said upper level wire comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire, at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level; and

said upper conductive liner in contact with said lower core conductor and also in contact with [the inner surface or the outer surface or] both the inner surface and the outer surface of said upper edge of said conductive liner in a liner-to-liner contact region.

10. (Twice amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and a via integrally formed in the bottom of said upper level wire, said via have a side and a bottom, said upper level wire and said via

each comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of said via, at least a portion of the bottom of said via extending below a top surface of said lower wire level; and

said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with [the inner surface or the outer surface or] both the inner surface and the outer surface of said upper edge of said lower conductive liner in a liner-to-liner contact region.

20. (Twice amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below the top surface of said lower wire level; and

said upper conductive liner on the bottom of each via of a first portion of said array of vias in contact with said lower core conductor and each via of a second portion of said array of

vias in contact with said lower core conductor and also in contact with [the inner surface or the outer surface or] both the inner surface and the outer surface of said upper edge of said lower conductive liner in liner-to-liner contact regions.

25. (Twice amended) An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom and one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire, said lower level wire and extensions comprising a lower core conductor and an lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire and said extensions, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below a top surface of said extensions of said lower wire level; and

said upper conductive liner on the bottom of each said via of a first portion of said array of vias in contact with said lower core conductor of said lower level wire and a second portion of said array of vias in contact with said lower core conductor of said extensions and also in contact with [the inner surface or the outer surface or] both the inner surface and the outer surface of said upper edge of said lower conductive liner of said extensions in liner-to-liner contact regions.